Circuit board — 10
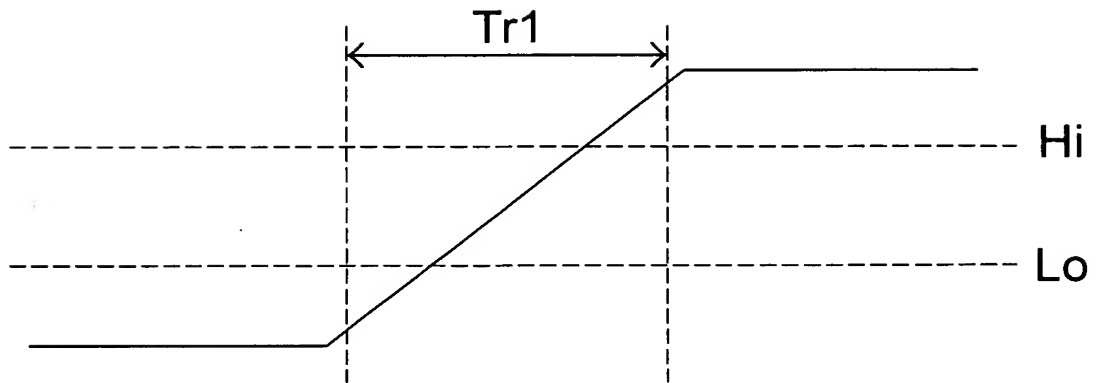
Source chip — 11
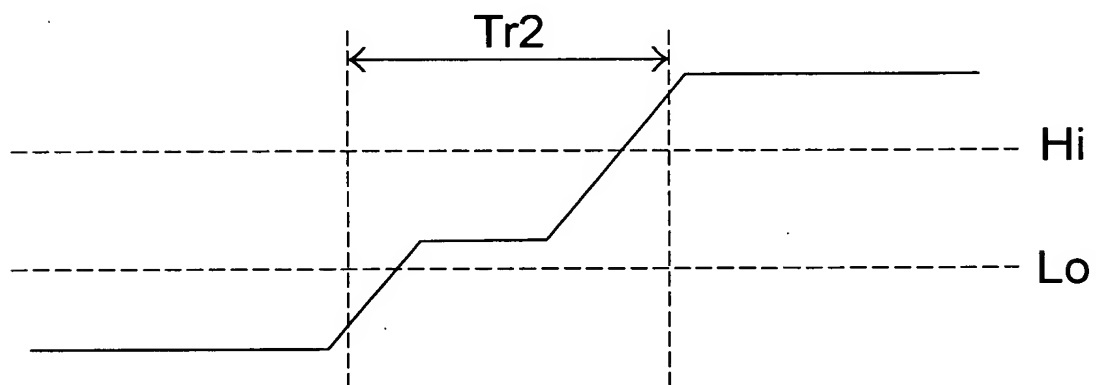
Destination chip — 12
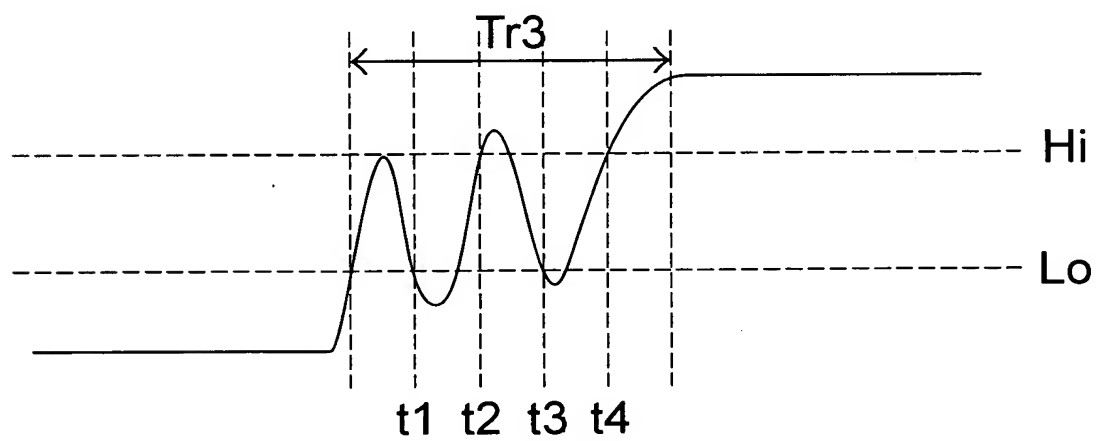
S1

13

Fig.1
PRIOR ART

Fig.2A
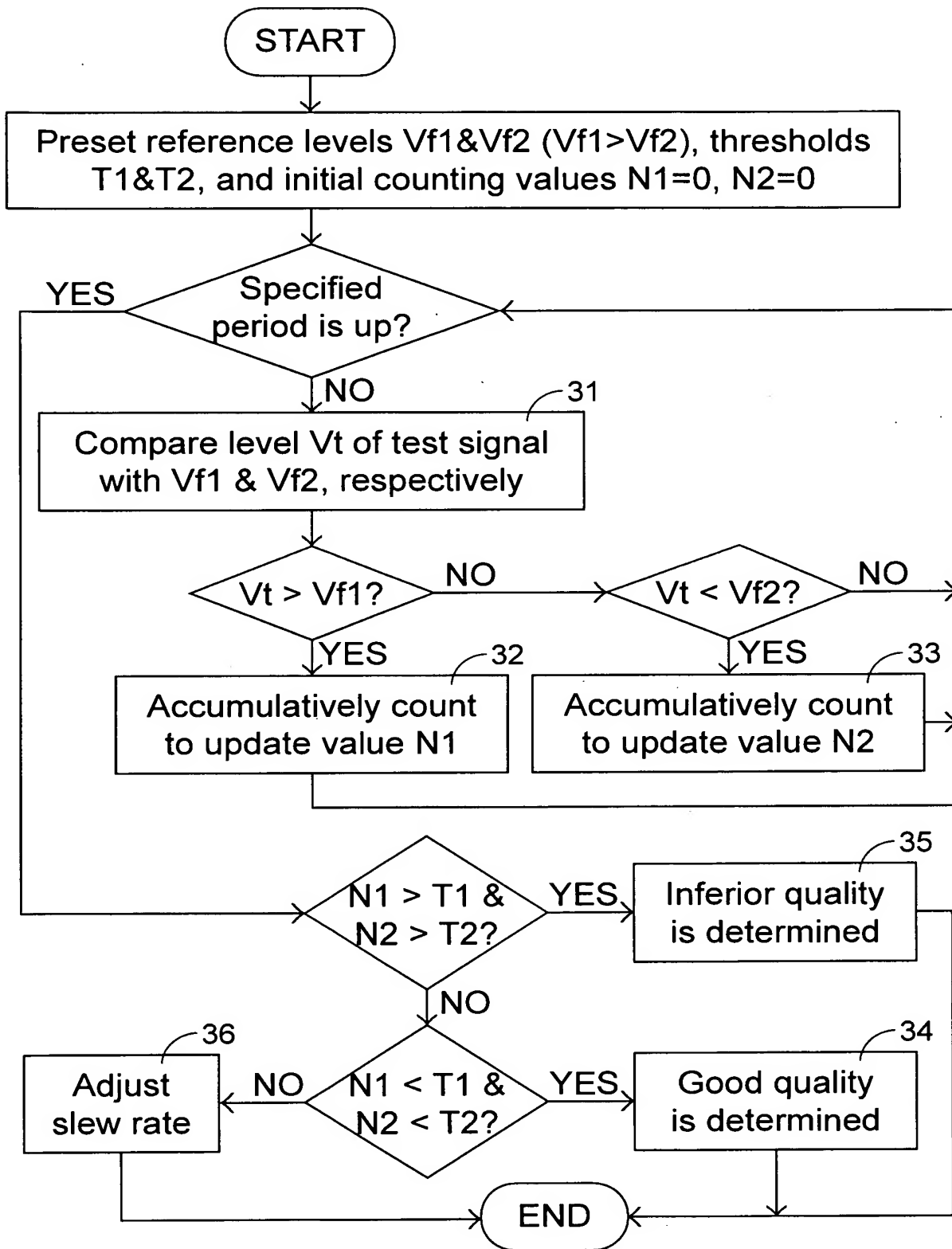PRIOR ART



Fig.2B
PRIOR ART



Fig.2C
PRIOR ART

START

Preset reference levels Vf1&Vf2 (Vf1>Vf2), thresholds T1&T2, and initial counting values N1=0, N2=0

YES ← Specified period is up?

NO

31 — Compare level Vt of test signal with Vf1 & Vf2, respectively

Vt > Vf1? —NO→ Vt < Vf2? —NO→

YES

32 — Accumulatively count to update value N1

YES

33 — Accumulatively count to update value N2

N1 > T1 & N2 > T2? —YES→ 35 — Inferior quality is determined

NO

36 — Adjust slew rate ←NO— N1 < T1 & N2 < T2? —YES→ 34 — Good quality is determined

END

Fig.3

Fig.4